REMARKS

The present amendment and request for reconsideration is filed in response to the final Office Action mailed August 2, 2005, the period of response having been extended to December 2, 2005. Claims 15-19 have been canceled. Claims 1-14 and 20-25 remain pending in the application.

In the Office Action, Claims 1 - 25 were rejected as being anticipated by Pierrat et al., U.S. Patent No. 6,854,609. The Examiner has pointed to Col. 5, lines 29-32 of the Pierrat reference as evidence that the reference discloses performing a simulation of the etch effects that would occur if a wafer is created using a mask/reticle corresponding to a first set of mask/reticle data. In addition, the Examiner cites FIGURE 7, elements 730, 740 and 750 as evidence that the reference discloses using etch biases in an OPC loop. Applicants again respectfully traverse the rejection.

The Pierrat reference discloses using either a rule-based OPC, a model-based OPC or a mixture of rule and model-based OPC to test and correct a semiconductor layout. See Col. 1, line 65- Col. 2, line 3. In the rule-based OPC, corrections are made based on a match between the geometry of the feature to be corrected and the particular rule defined. See Col. 5, lines 30-67. In model-based OPC, a mathematical model of the manufacturing process is used to make the corrections. As was pointed out by the Examiner, the mathematical model may handle various effects including dry or wet etching effects.

What is not disclosed in the Pierrat reference is *first* compensating the layout data for etch effects *and then* analyzing the compensated layout data with a model-based OPC tool to correct for optical/resist process distortions. In the mixed mode processing described at Col. 6, lines 47-59, the Pierrat reference says that the layout may be compensated with a rule-based OPC followed by a model-based OPC. In some embodiments, the layout is pre-biased (see Col. 8,

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lines 15-21). However, there is no teaching or suggestion in the Pierrat reference that such pre-bias compensates for expected etch effects that would occur if a layout is printed on a wafer. Similarly, although the Pierrat reference does teach that the mathematical model of the OPC tool can handle etch effects, nothing suggests that the model would incorporate *previously* calculated etch effects in the OPC loop. Etch processes typically follow lithographic imaging processes and therefore are usually modeled in the sequence in which they occur. Modeling and compensating for etch effects before compensating for imaging effects is not taught or suggested in the Pierrat reference.

With respect to Claim 1, the applicants submit that nothing in the cited Pierrat references teaches or suggests the claimed combination of acts including using the results of an etch simulation to compensate features within a set of mask/reticle data for etch distortions that would occur during lithographic processing; and performing optical process correction (OPC) to compensate for optical/resist process distortions using the etch compensated set of mask/reticle data as an input.

Similarly with respect to Claim 5, the applicants submit that nothing in the cited Pierrat references teaches or suggests the claimed combination of acts including performing a simulation of the etch effects that would occur if a wafer is created using a mask/reticle corresponding to the set of mask/reticle data; calculating etch biases from the etch simulation result; and applying the previously calculated etch biases within a model-based optical process correction (OPC) loop that adjusts the mask/reticle data for optical/resist process distortions.

Because the Pierrat reference does not disclose at least these features of Claim 1 and 5, it is submitted that these claims, as well as the claims that depend thereon, are allowable. In addition, Claims 8, 12, 20 and 23, as well as the claims that depend thereon, are allowable for the same reasons as set forth above.

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In light of the above, it is submitted that all claims are in condition for allowance. It is therefore requested that the Examiner withdraw the rejections and pass this case to issue at the earliest possible date.

If the Examiner has any additional questions, he is invited to contact the undersigned attorney at the telephone number provided below.

Respectfully submitted,

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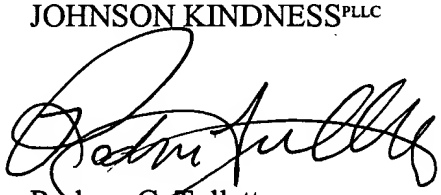

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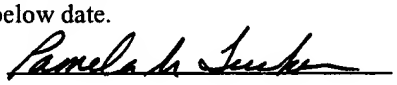
Date: December 2, 2005 

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